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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/456,873	12/08/1999	SEIICHI MORI	005702-20053	7026

26021 7590 05/22/2002

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EXAMINER
ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AE

Office Action Summary	Application No. 09/456,873	Applicant(s) MORI, SEIICHI
	Examiner Leonardo Andújar	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

FREDERICK L. ABRAHAM
PRIMARY EXAMINER

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 03/08/2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/456873 is acceptable and a CPA has been established. An action on the CPA follows.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 12/09/1998. The certified copy of the priority document has been received.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The present invention is directed to an inter insulating layer comprising a second insulating layer having a lower trap density than that of a first

silicon insulating layer. However, a proper definition of trap density has not been provided. Additionally, no information or relevant literature that states the effect of the trap density in the physical or electrical properties of silicon nitride has been provided. A definition within the context of the present application is required.

6. Claims 5 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The phrase "an ordinary trap density obtained by typical CVD condition" in claims 5 and 9 is a relative term, which renders the claim indefinite. The phrase " a lower trap density than an ordinary trap density obtained by typical CVD" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The specification does not contain any disclosure regarding an actual magnitude or range of trap density typical for silicon nitride layers obtained by CVD.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Initially, and with respect to claims 1, 2, 5 - 10, 12, 13, 15, 17 and 18 note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279,

26 USPQ 57, 61 (2d. Cir. 1935). **Note that Applicant has burden of proof in such cases** as the above case law makes clear.

11. Claims 5, 6, 9-13 are rejected under 35 U.S.C. § 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Takeuchi (US 5, 907, 183).

12. Regarding claims 5 and 6 (as understood), Takeuchi (e.g. fig. 1) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate 11;
- And a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the semiconductor substrate, and a control gate 15 provided through an inter-layer insulating layer 14 on the floating gate.

13. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer contiguous to the floating gate and a silicon nitride deposited on the silicon oxide layer (col. 1/lls. 37-55). As to the grounds of rejection under section 103(a), the method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the final device. See MPEP § 2113, which discusses the handling of "product by process" claims and recommends the alternative (§ 102 / § 103) grounds of rejection.

14. Regarding claims 9 and 10 (as understood), Takeuchi (e.g. fig. 2b) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate;

- And a memory cell having a floating gate 23 provided through a tunnel insulating layer 22 on the semiconductor substrate, and a control gate 28 provided through an inter-layer insulating layer 27 on the floating gate.

15. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon nitride layer 24 contiguous to the floating gate. As to the grounds of rejection under section 103(a), the method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the final device. See MPEP § 2113, which discusses the handling of "product by process" claims and recommends the alternative (§ 102 / § 103) grounds of rejection.

16. Regarding claim 11, Takeuchi discloses a second nitride layer 26. The first silicon nitride layer and the second nitride layer are so double layered as to be continuous to both the floating gate and the control gate. Also, Takeuchi discloses a silicon oxide 25 layer interposed between the double-layered silicon nitride layers (col. 6/lls. 42-53).

17. Regarding claim 12, Takeuchi (e.g. 9) discloses a first and second nitride layer (72, 76). The first silicon nitride layer and the second nitride layer are so double layered as to be continuous to both the floating gate and the control gate. Also, Takeuchi discloses a silicon oxide 73 layer and a silicon nitride layer 74 interposed between the double-layered silicon nitride layers (col. 9/lls. 1-7).

18. Regarding claim 13, Takeuchi (e.g. 9) shows that the silicon nitride layer 72 is provided only on the side contiguous to the floating gate. Also, Takeuchi discloses a

silicon oxide 73 layer and a stacked layer (74, 75, 76) consisting of silicon nitride layer and a silicon oxide layer provided on the silicon nitride (col. 9/lls. 1-7).

19. Claims 1-4, 7-8 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeuchi in view of Cavins et al. (US 5,731,238).

20. Regarding claims 1 and 2 (as understood), Takeuchi (e.g. fig. 9) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate;
- And a memory cell having a floating gate 23 provided through a tunnel insulating layer 22 on the semiconductor substrate, and a control gate 28 provided through an inter-layer insulating layer 71 on the floating gate.

21. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer 73 contiguous to the floating gate, a first silicon nitride 74 (conventional SiN) deposited on the silicon oxide layer and a second silicon nitride layer (col. 9/lls. 1-7). Additionally, the method for depositing the silicon nitride layers e.g. JVD, is an intermediate process step that does not affect the structure of the final device. However, Takeuchi does not disclose that the second silicon nitride layer has a lower trap density than that of the first silicon nitride layer. Cavins discloses a non volatile memory device that includes a silicon nitride inter insulating layer 21 having a trap density lower than the conventional trap density (col.4/lls. 13-23). Moreover, Cavins discloses that this type of silicon nitride layer is used to improve the device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

make the second silicon nitride layer of Takeuchi having a lower trap density than the conventional silicon nitride trap density in order to improve the electrical performance of the device as taught by Cavins.

22. Claim 2 does not distinguish over the Takeuchi in view Cavins references regardless of the process used to make the silicon nitride layer, because only the final product is relevant, not the process of making such as JVC. Note that a "product by process" claim is directed to the product per se, no matter how actually made (see comments above).

23. Regarding claim 3, Cavins discloses that hydrogen quantity of a conventional silicon nitride may be more than $10^{21}/cm^3$ (col.6/lls. 23-31).

24. Regarding claim 4, Cavins discloses that hydrogen quantity of a conventional silicon nitride is close to $10^{19}/cm^3$ (col.4/lls. 15-16).

25. Regarding claims 7 and 8, Takeuchi (e.g. fig. 1) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate 11;
- And a memory cell having a floating gate 13 provided through a tunnel insulating layer 12 on the semiconductor substrate, and a control gate 15 provided through an inter-layer insulating layer 14 on the floating gate.

26. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon oxide layer contiguous to the floating gate and a silicon nitride deposited on the silicon oxide layer (col. 1/lls. 37-55). Additionally, the method for depositing the silicon nitride layer e.g. JVD, is an intermediate process step that does not affect the structure of the

final device. However, Takeuchi does not disclose that the silicon nitride layer have a hydrogen content of $10^{19}/cm^3$ or less. Cavins discloses a non volatile memory device that includes a silicon nitride inter insulating layer 21 having a hydrogen content of $10^{19}/cm^3$ or less (col. 5/lls. 7-8; col. 6/lls. 27-29). Moreover, Cavins discloses that this type of silicon nitride layer is used to improve the device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the silicon nitride layer of Takeuchi having a hydrogen content of $10^{19}/cm^3$ or less in order to improve the electrical performance of the device as taught by Cavins.

27. Claim 8 does not distinguish over the Takeuchi in view Cavins references regardless of the process used to make the silicon nitride I layer, because only the final product is relevant, not the process of making such as JVC. Note that a "product by process" claim is directed to the product per se, no matter how actually made (see comments above).

28. Regarding claim 14, Takeuchi (e.g. fig. 2b) shows a non volatile semiconductor memory device comprising:

- A semiconductor substrate;
- And a memory cell having a floating gate 23 provided through a tunnel insulating layer 22 on the semiconductor substrate, and a control gate 28 provided through an inter-layer insulating layer 27 on the floating gate.

29. Also, Takeuchi discloses that the inter-layer insulating layer includes a silicon nitride layer 24 contiguous to the floating gate. However, Takeuchi does not disclose

that the silicon nitride layer have a hydrogen content of $10^{19}/cm^3$ or less. Cavins discloses a non volatile memory device that includes a silicon nitride inter insulating layer 21 having a hydrogen content of $10^{19}/cm^3$ or less (col. 5/lls. 7-8; col. 6/lls. 27-29). Moreover, Cavins discloses that this type of silicon nitride layer is used to improve the device electrical performance and to reduce the manufactures cost (col. 6/lls. 57-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the silicon nitride layer of Takeuchi having a hydrogen content of $10^{19}/cm^3$ or less in order to improve the electrical performance of the device as taught by Cavins.

30. Claim 15 does not distinguish over the Takeuchi in view Cavins references regardless of the process used to make the silicon nitride I layer, because only the final product is relevant, not the process of making such as JVC. Note that a "product by process" claim is directed to the product per se, no matter how actually made (see comments above).

31. Regarding claim 16, Takeuchi discloses a second nitride layer 26. The first silicon nitride layer and the second nitride layer are so double layered as to be continuous to both the floating gate and the control gate. Also, Takeuchi discloses a silicon oxide 25 layer interposed between the double-layered silicon nitride layers (col. 6/lls. 42-53).

32. Regarding claim 17, Takeuchi (e.g. 9) discloses a first and second nitride layer (72, 76). The first silicon nitride layer and the second nitride layer are so double layered as to be continuous to both the floating gate and the control gate. Also, Takeuchi

discloses a silicon oxide 73 layer and a silicon nitride layer 74 interposed between the double-layered silicon nitride layers (col. 9/lls. 1-7). Regarding the process used to make the silicon nitride layer, it is noted that only the final product is relevant, not the process of making such as CVD. Note that a "product by process" claim is directed to the product per se, no matter how actually made (see comments above).

33. Regarding claim 18, Takeuchi (e.g. 9) shows a silicon nitride layer 72 provided only on a side contiguous to the floating gate. Also, Takeuchi discloses a silicon oxide 73 layer and a stacked layer (74, 75, 76) consisting of silicon nitride layer and a silicon oxide layer provided on the silicon nitride (col. 9/lls. 1-7).

Response to Arguments

34. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 5:00 PM (Eastern Standard Time) Monday through Friday or by e-

mail via Leonardo.Andujar@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

37. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

38. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/314-317, 324,325, 406, 410	05/02
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	05/02

Leonardo Andújar
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5/13/02

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PRIMARY EXAMINER